IN THE CLAIMS:

1. (Currently Amended) A data driver outputting a plurality of analog grayscale voltages to a plurality of data bus lines, comprising:

a grayscale voltage generating portion generating the plurality of analog grayscale voltages for a predetermined number of grayscales;

a selector portion provided for each of the data bus lines and selecting any one of the plurality of analog grayscale voltages based on grayscale data;

a plurality of grayscale voltage lines connected to the grayscale voltage generating portion and provided for each of the plurality of analog grayscale voltages and supplying the analog grayscale voltages to the selector portion; and

a switching portion electrically disconnecting the plurality of grayscale voltage lines from the grayscale voltage generating portion during an operation test and electrically connecting the plurality of grayscale voltage lines to the grayscale voltage generating portion during a normal mode of operation.

2. (Original) A data driver according to Claim 1, wherein the grayscale voltage generating portion has a ladder resistor portion which has a plurality of resistors connected in series and which generates the plurality of analog grayscale voltages through resistance division.

3. (Original) A data driver according to Claim 1, wherein the grayscale voltage generating portion has a ladder resistor portion which has a plurality of

transistors connected in series and which generates the plurality of analog grayscale voltages through resistance division utilizing on-resistances of the transistors.

4. (Original) A data driver according to Claim 1, comprising a state setting circuit setting each of the plurality of grayscale voltage lines at a "High" level or a "Low" level independently during the operation test.

5. (Original) A data driver according to Claim 4, wherein the state setting circuit maintains ends of the plurality of grayscale voltage lines in a high impedance state during a normal operation.

6. (Original) A data driver according to Claim 5, wherein the state setting circuit is provided at ends of wiring of the plurality of grayscale voltage lines opposite to the grayscale voltage generating portion.

7. (Original) A data driver according to Claim 6, wherein the state setting circuit has:

a plurality of switching elements for state switching having a CMOS structure whose output ends are connected to the end of wiring of each of the plurality of grayscale voltage lines; and

a plurality of state switching circuits which are connected to input ends of the switching elements for state switching and which set the output state of each of the plurality of switching elements for state switching in a "High", "Low" or "Hiz" state.

8. (Original) A data driver according to Claim 7, comprising a testing control portion which controls the state setting circuit during the operation test to sequentially set the plurality of grayscale voltage lines at the "High" level one at a time.

9. (Original) A data driver according to Claim 4, wherein the state setting circuit has a plurality of switching elements for state switching which are respectively connected to the plurality of grayscale voltage lines between the grayscale voltage generating portion and the selector portion.

10. (Original) A data driver according to Claim 9, comprising a testing control portion which controls the state setting circuit during the operation test to sequentially set the plurality of grayscale voltage lines at the "High" level one at a time.

11. (Original) A display having a plurality of data bus lines and displaying images, comprising a data driver according to any one of Claims 1 through 10 which outputs an analog grayscale voltage to the plurality of data bus lines.